UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,478	03/31/2004	James Loran Ball	ALTRP134/A1466	6370

22434 7590 04/08/2005

BEYER WEAVER & THOMAS LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/815,478	BALL, JAMES LORAN	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,9 and 11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,9 and 11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 22, 2005 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1 – 4, 7, 9 and 11 – 19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 1 and 19 are objected to because of the following informalities: In claim 1, line 2 from the bottom, the word "a" following the phrase "plasma treatment' should be deleted. In claim 19, in line 5, the phrase "the anti-diffusion film" following the phrase "stacked on' should be replaced by "the polysilicon film". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1 – 3, 7, 9- 12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky, US 5,412,246 in view of Mandelman, US 6,720,630, Chau, US 2002/0053711 and Wolf, "Silicon processing For The VLSI Era", Vol. 1, p. 520, Lattice Press (1986).

Regarding claim 1, Dobuzinsky teaches a method of forming a gate in a semiconductor device, comprising the steps of:

- forming a gate pattern on a gate oxide film 32 and a conductive

layer 34 are stacked at a give region on a semiconductor substrate 30 with reference to Fig. 4A;

- forming a hard mask 36 on top of the gate pattern; and
- performing oxygen plasma treatment to form oxide film 38 on sides of the conductive layer 34 and not on the hard mask 36 with reference to Fig. 4B in column 6, lines 30 – 55.

Dobuzinsky fails to teach the gate pattern includes 1) a polvsilicon film, an anti-diffusion film stacked on the polysilicon film and a metal film stacked on the anti-diffusion film and 2) wherein a cleaning process using a HF solution is performed on the polysilicon film before the anti-diffusion film is stacked thereon to remove a native oxide from the polysilicon film.

Regarding element 1), Mandelman teaches forming a gate stack comprising, a polysilicon film, an anti-diffusion film of TaSiN or WN, a metal film of W and a hard mask of nitride for the benefit of providing a diffusion free low resistivity gate structure for MOSFET devices with reference to Fig. 2 and in column 4, lines 13 – 62.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Dobuzinsky and form the gate stack comprising, a polysilicon film, an anti-diffusion film of TaSiN or WN, a metal film of W and a hard mask of nitride for the benefit of providing a diffusion free low resistivity gate structure for MOSFET devices as taught by Mandelman in column 4, lines 13 – 62.

Regarding element 2), Chau teaches the removal of native oxide by HF solution before forming a low resistance silicide film on the polysilicon layer in paragraph 51.

Wolf also teaches the removal of native oxide from silicon surface for the benefit of enhancing further processing steps by reducing the contact resistance within interfacial layers (see 2nd paragraph in page 520).

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Dobuzinsky and form the antidiffusion film on the polysilicon film after a cleaning process using a HF solution to remove a native oxide from the polysilicon film for the benefit of forming a low resistance contact between the polysilicon and the anti-diffusion film as taught by Chau in paragraph 51 and Wolf (see 2nd paragraph in page 520) so that a low resistivity gate structure is assured.

Regarding claims 2 and 3, Dobuzinsky teaches gate oxide film of silicon oxide in column 6, lines 55 – 60.

Regarding claims 7 and 9, Mandelman teaches forming a gate stack comprising, an anti-diffusion film of TaSiN or WN, a metal film of W for the benefit of providing a diffusion free low resistivity gate structure for MOSFET devices with reference to Fig. 2 and in column 4, lines 13 – 62 as described easrlier in rejecting claim 1.

Regarding claim 11, Dobuzinsky teaches plasma treatment by applying the RF source power of 100 - 3000W and RF bias power of 0 – 100 W in column 6, lines 45 – 55.

Regarding claim 12, Dobuzinsky teaches plasma treatment by oxygen in column 6, lines 45 – 55.

Regarding claim 15, Dobuzinsky teaches plasma treatment at substrate temperature of 0 – 450 °C in column 6, lines 45 – 55.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky, US 5,412,246 in view of Mandelman, US 6,720,630, Chau, US 2002/0053711 and Wolf, "Silicon processing For The VLSI Era", Vol. 1, p. 520, Lattice Press (1986) as applied to claim 2 above, and further in view of Lin, US 6,746,925.

Dobuzinsky in view of Mandelman, Chau and Wolf fails to teach high dielectric metal oxide films.

Lin teaches gate dielectric metal oxide films of HfO_2 for the benefit of retaining the electrical characteristics of thin gate dielectric layer in column 3, lines 15 – 67.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Dobuzinsky and form gate oxide film with high dielectric metal oxide film such as HfO_2 for the benefit of retaining the electrical characteristics of thin gate dielectric layer as taught by Lin in column 3, lines 15 – 67.

9. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky, US 5,412,246 in view of Mandelman, US 6,720,630, Chau, US 2002/0053711 and Wolf, "Silicon processing For The VLSI Era", Vol. 1, p. 520, Lattice Press (1986) as applied to claims 1 and 11 above, and further in view of Kashiwagi, US 6,297,172.

Dobuzinsky in view of Mandelman, Chau and Wolf fails to teach plasma treatment performed using oxygen and hydrogen in a flow ratio of 0.01 ~ 0.2.

Kashiwagi teaches plasma oxidation using oxygen and hydrogen in column 9, lines 65 – 67 for the benefit of providing very thin oxide film with excellent reliability in column 18, lines 50 – 51.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Dobuzinsky and form the oxide film by plasma oxidation using oxygen and hydrogen for the benefit of providing very thin oxide film with excellent reliability as taught by Kashiwagi in column 18, lines 50 – 51

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky, US 5,412,246 in view of Mandelman, US 6,720,630, Chau, US 2002/0053711 and Wolf, "Silicon processing For The VLSI Era", Vol. 1, p. 520, Lattice Press (1986) as applied to claims 1 above, and further in view of Kizilialli, US 6,320,238.

Dobuzinsky in view of Mandelman, Chau and Wolf fails to teach implementing the oxygen plasma treatment by illuminating ultraviolet rays on the top of the substrate.

Kizilialli teaches illuminating ultraviolet rays to activate the ozone, which can used for the plasma oxidation process as well-known process in column 4, lines 41 – 50.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Dobuzinsky and implement the oxygen plasma treatment by illuminating ultraviolet rays on the top of the substrate by supplying ozone as an oxidizing gas taught by Kizilialli as well-known in the art in column 4, lines 41 – 50.

11. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky, US 5,412,246 in view of Mandelman, US 6,720,630, Chau, US 2002/0053711 and Wolf, "Silicon processing For The VLSI Era", Vol. 1, p. 520, Lattice Press (1986) as applied to claims 1 above, and further in view of Kizilialli, US 6,320,238 and Misra, US 6,274,429.

Dobuzinsky in view of Mandelman, Chau and Wolf fails to teach annealing process for the plasma formed oxide film.

Kizilialli teaches annealing of the oxide film in nitrogen atmosphere at a temperature of 600 ~ 1000°C for the benefit of providing a stress free film in column 4, lines 61 – 65.

Misra teaches oxide annealing for a time of 10 sec ~ 60 min for the benefit of providing good electrical quality to oxide film in column 4, lines 15 – 39.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Dobuzinsky and perform an annealing process for plasma deposited oxide film in nitrogen atmosphere at a temperature of 600 ~ 1000°C for a time of 10 sec ~ 60 min for the benefit of providing a stress free film as taught by Kizilalli in column 4, lines 61 – 65 and for the benefit of providing good electrical quality to oxide film as taught by Misra in column 4, lines 15 – 39.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky, US 5,412,246 in view of Mandelman, US 6,720,630; Chau, US 2002/0053711; Wolf, "Silicon processing For The VLSI Era", Vol. 1, p. 520, Lattice Press (1986); Kizilialli, US 6,320,238 and Misra, US 6,274,429.

Limitations of this claim have been described earlier in rejecting claims 1, 17 and 18.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar
Asok K. Sarkar
April 6, 2005

Primary Examiner